3. (Amended) A method according to claim 1 further including adjusting the bias current, thereby adjusting the input impedance of the cell.

4. A method according to claim 1 wherein biasing the transistor cell includes:

coupling a bias signal to the base of the grounded base transistor; and

varying the bias signal with temperature such that it causes the bias current through the grounded base transistor and the current mirror to be proportional to absolute temperature.

5. A method according to claim 1 wherein:

the current mirror is coupled to a power supply terminal; and

biasing the transistor cell includes maintaining the base of the grounded base transistor at about $2V_{BE}$ from the voltage of the power supply terminal.

6. A method according to claim 1 further including isolating the current mirror from the output terminal.

7. A method according to claim 6 wherein isolating the current mirror includes coupling a cascode transistor between the output terminal and the current mirror.

8. (Amended) A squaring cell comprising:

an input terminal;

an output terminal;

a grounded base transistor coupled between the input and output terminals;

a current mirror coupled between the input and output terminals; and

a bias signal generator coupled to the grounded base transistor to establish a bias current through the grounded base transistor and the current mirror, wherein the bias signal generator generates a bias signal that varies with temperature such that it causes the bias current through each of the transistors to be proportional to absolute temperature.

9. A squaring cell according to claim 8 further including a cascode transistor coupled between the current mirror and the output terminal.

10. A squaring cell according to claim 8 wherein the current mirror is coupled to a power supply terminal, and the bias signal generator maintains the base of the grounded base transistor at about $2V_{BE}$ from the voltage of the power supply terminal.

11. A squaring cell according to claim 8 wherein the current mirror includes:

a diode-connected transistor coupled between the input terminal and a power supply terminal; and

a mirror transistor having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

12. A squaring cell according to claim 8 wherein:

the grounded base transistor has a collector coupled to the output terminal, a base for receiving the bias signal, and an emitter coupled to the input terminal;

the current mirror includes:

a diode-connected transistor having a collector and base coupled to the input terminal and an emitter coupled to a power supply terminal, and

a mirror transistor having a collector coupled to the output terminal, a base coupled to the input terminal, and an emitter coupled to the power supply terminal.

13. (Cancelled)

14. A squaring cell according to claim 8 wherein the bias signal generator includes:

two diode-connected transistors coupled in series between the input terminal and a power supply terminal; and

a current source coupled to the diode connected transistors to cause a bias current to flow through the diode connected transistors.

Please add new claim 15 as follows.

15. (New) A method according to claim 1 wherein limiting the input signal to a range in which the output function of the transistor cell approximates a square-law ccmprises limiting the input signal to less than about four times the bias current.